US-PAT-NO: **6271117**

DOCUMENT-IDENTIFIER: US 6271117 B1

TITLE: Process for a nail shaped landing pad plug

---------- KWIC ---------

The invention has two embodiments for forming a **contact plug** having large nail shaped landing pad. The large pad areas increase the overlay tolerances. The first embodiment comprises forming first 20 and **second** 24 **insulating** layers over a semiconductor structure. A first photoresist layer 28 with a first opening is formed over the **second insulating** layer 24. The **second insulating** layer 24 is isotropically etched using an etchant with a high selectivity thereby forming a disk shaped opening 26A. The disk shaped opening is used to define the large nail shaped landing pad. The first **insulating** layer 20 is etched using a dry etch thereby forming a nail shaped contact opening 26. The opening is filled with polysilicon to form the nail shaped conductive plug 36. The **second** embodiment begins by forming a first **insulating** layer 40 over a semiconductor structure. A first photoresist layer 44 with a first opening is formed over the first **insulating** layer 24. The first **insulating** layer is isotropically etched to form a half spherical hole. The first **insulating** layer 40 is then anisotropically etched; and forming a rounded nail shaped contact hole 50. The hole 50 is filled thereby forming the rounded nail shaped conductive plug 58.

To accomplish the above objectives, the present invention provides two preferred embodiments for manufacturing a nail shaped landing pad plug. The first embodiment (FIGS. 1A-4C) uses two **insulating** layers with different etch

rates. A lateral portion of the top **insulating** layer 24 is etched to form a mold for the flat large landing pad 36. The **second** embodiment (FIGS. 5-8) uses one **insulating** layer that is etched with two etches--(1) isotropic etch and (2) anisotropic etch. The isotropic etch forms a half spherical shaped hole (e.g., bowl shaped) which is used to form the rounded head of the rounded nail shaped landing pad 58.

a) (See FIG. 1) forming a first **insulating** layer 20 composed of an oxide over a contact area on a semiconductor structure;

b) forming a **second insulating** layer 24 composed of an oxide over the first **insulating** layer 20;

c) forming a first photoresist layer 28 over the **second insulating** layer 24; the first photoresist layer 28 having a first photoresist opening over the contact area;

d) **etching the second insulating** layer 24 using an isotropic etch having a selectivity in a range of between about 2:1 and 20:1 between the **second insulating** layer 24 and the **first insulating** layer 20; the isotropic etch **removing** a width 25 of the **second insulating** layer in said first photoresist opening 28A in a range of between about 0.05 and 0.3 .mu.m;

e) **etching the first insulating** layer 20 using a dry etch to expose the surface of the substrate 10;

The **second** embodiment of the present invention forms a rounded nail shaped plug using a two step etch. The method of the **second** embodiment comprises:

(See FIG. 5) forming a first **insulating** layer 40 composed of an oxide over a semiconductor structure;

forming a first photoresist layer 44 over the first **insulating** layer 40; the

first photoresist layer 28 having a first photoresist opening over the contact area;

performing a first etch on the first **insulating** layer 40 using an isotropic etch;

performing a **second** etch the first **insulating** layer 40 using an anisotropic etch **exposing** the surface of the **substrate** 10; the **second** etch forming a rounded nail shaped contact hole 26;

FIGS. 5 through 8 are cross sectional views for illustrating a **second** embodiment of method for manufacturing a rounded nail shaped landing pad poly plug according to the present invention.

FIGS. 9A and 9B show top down views of the nail shaped plug of the first and **second** embodiments of the present invention.

The method of the first embodiment is shown in FIGS. 1A to 4C. As shown in FIG. 1A, a first **insulating** layer 20 is formed over a semiconductor structure 10. The semiconductor structure can comprise layers and devices formed over and in a substrate. The semiconductor structure can include semiconductor devices, such as field effect transistors (FETs) that comprise gates 12, gate **insulating** layers 14, spacers 16, gate **dielectric** layers 18, etc. The substrate has a contact area 11 over an active region. The plug 36 will be formed contacting the contact area 11.

The first **insulating** layer 20 can be composed of a oxide, or a TEOS oxide and is more preferably composed of TetraEthylOrthoSilicate (TEOS) oxide. The first **insulating** layer 20 preferably has a thickness in a range of between about 1000 and 2000 .ANG..

Next, a **second insulating** layer 24 is formed over the first **insulating** layer 20. The **second insulating** layer preferably has an etch selectivity of between

about 2:1 and 20:1 between the **second insulating** layer 24 and the first **insulating** layer 20 and more preferably an etch selectivity of about 10:1.

The **second insulating** layer 24 preferably composed f an oxide such as PE-Oxide, borophosphosilicate glass(BPSG) or hosphosilicate glass (PSG) and is more preferably composed of PE-Oxide.

The preferred combination of the first and **second insulating** layer and isotropic etches are shown below in table 1.

Still referring to FIG. 1A, a first photoresist layer 28 is formed over the **second insulating** layer 24. The first photoresist layer 28 preferably has a first photoresist opening over the contact area 11. The first photoresist opening preferably has an open dimension (e.g., diameter) in a range of between about 0.15 and 2.0 .mu.m and more preferably between 0.15 and 0.5 .mu.m. The first photoresist opening can have any shape, such as circular, rectangular, square or triangular, and is more preferably circular shaped.

As shown in FIG. 2A, the **second insulating** layer 24 is preferably etched through the first photoresist opening using an isotropic etch having a selectivity in a range of between about 2:1 and 20:1 between the **second insulating** layer 24 and the first **insulating** layer 20. The isotropic etch of the **second insulating** layer preferably comprises a Buffered oxide etch (BOE) or Dilute HF (DHF) and the isotropic etch removes a width 25 of the **second insulating** in a range of between about 0.05 and 0.3 .mu.m. The isotropic etch forms a disk shape opening 26A (e.g., upper opening or landing pad opening) that is used to shape (e.g., mold) the large landing pad of the plug 36.

The first **insulating** layer 20 is then etched using a dry etch (e.g., an anisotropic etch) to expose the surface of the substrate 10. The etch forms the lower opening 26B. The combination of the upper 26A and the lower 26B opening form the nail shaped opening 26 that will be used to form the nail shaped plug. The first photoresist layer 28 is then removed.

As shown in FIG. 4C, a next overlying level of metal contact/metal layer 37 can be formed contacting the large rounded nail shaped landing pad 36 of the plug of the invention. A **dielectric** layer 21 is formed over the **second insulating** layer 24. The **dielectric** layer 21 is patterned. A metal layer 37 is formed contacting the large landing pad plug 36. The metal layer is then patterned. As shown in FIG. 4D, the overlying conductive layer 37 be another nail shaped landing pad plug 3638 of the invention.

The **second** embodiment of the invention forms a rounded nail shaped plug 58 of a semiconductor device. FIGS. 5 through 8 show the sequence of steps for the **second** embodiment.

Turning to FIG. 5, a first **insulating** layer 40 is formed over a semiconductor structure. The semiconductor structure 10 can formed over a silicon substrate. The first **insulating** layer 40 is preferably composed of an oxide (BPSG or undoped silicon glass (USG)) and more preferably composed of borophosphosilicate glass. A contact area where the plug will contact the substrate is preferably defined over an active region in the substrate. The **contact plug** 58 can be formed over a substrate or another conductive layer.

As shown in FIG. 5, a first photoresist layer 44 is formed over the first **insulating** layer 24. The first photoresist layer 44 has a first photoresist opening 44A over the contact area. The first photoresist opening can have any shape and preferably has a circular or rectangular shape and more preferably has a circular shape.

Still referring to FIG. 5, a first etch is performed on the first **insulating** layer 40 using an isotropic etch. The isotropic etch preferably comprises BOE or dilute HF (DHF). The first etch preferably removes a radius 47 of the first **insulating** layer 40 (in the first opening 46) in a range of between about 0.05 and 0.3 .mu.m. The etch forms a half bowl shaped hole that is used to define the landing pad area of the rounded nail shaped plug.

FIG. 5 shows a **second** etch is performed on the first **insulating** layer 40 using an anisotropic etch. The anisotropic etch exposes the surface of the substrate 10 in the lower opening 48. The **second** etch forms a rounded nail shaped contact hole 50 (4648) which is a combination of the upper bowl shaped opening 46 and the lower opening 48.

Next, as shown in FIG. 8, a conductive (e.g., metal contact/metal) layer 64 is formed contacting the large landing pad of the plug 58 of the invention. A **dielectric** layer 62 is formed over the first **insulating** layer 40. The **dielectric** layer is patterned. A metal layer 64 is formed contacting the large landing pad plug 58. The metal layer is then patterned.

Top down views of the first and **second** embodiments are shown in FIGS. 9A and 9B. FIG. 9A shows a circular plug 65 (36 or 58) and FIG. 9B shows a rectangular shaped plug 65 (36 or 58). The dashed line is the lower opening 26B or 48. The plug can have any shape. This plug is preferably circular, square or rectangular shaped.

TABLE 1 Preferred combinations of the invention. 1.sup.st **insulating** 2.sup.nd **Insulating** Combination layer 20 layer 24 Isotropic etch 1 TEOS BPSG BOE 2 TEOS PE-Oxide BOE or DHF 3 TEOS PSG BOE or DHF

a) forming a gate and an overlying gate **dielectric** layer over a semiconductor structure; forming a first **insulating** layer over said gate **dielectric** layer; said first **insulating** layer is composed of a TEOS oxide; planarizing said first **insulating** layer;

b) forming a **second insulating** layer on said first **insulating** layer; said **second insulating** layer is composed of a material selected from the group consisting of PSG; then

c) forming a first photoresist layer on said **second insulating** layer; said

first photoresist layer having a first photoresist opening over said contact area; then

d) **etching said second insulating** layer using an isotropic etch forming a disk shaped opening, said disk shaped opening having flat bottom comprised of said **first insulating** layer; said disk shape opening having sidewalls; the isotropic etch having an etch selectivity between said **second insulating** layer and said first **insulating** layer in a range of between about 2:1 and 20:1; then

e) **etching said first insulating** layer and said gate **dielectric** layer to form a lower opening; the etch using an anisotropic etch to expose the surface of said semiconductor structure; a nail shaped contact hole is comprised of (a) said disk shaped opening and (b) said lower opening; said lower opening having straight sidewalls; then

g) depositing a conductive layer filling said nail shaped contact hole and overlying said **second insulating** layer; and

2. The method of claim 1 wherein said first **insulating** layer has a thickness in a range of between about 1000 and 20,000 .ANG..

4. The method of claim 1 wherein the isotropic etch of said **second insulating** layer comprises a buffered oxide etch and the isotropic etch removes a width of said **second insulating** layer in said disk shaped opening in a range of between about 0.05 and 0.3 .mu.m.

a) forming a gate and an overlying gate **dielectric** layer over a semiconductor structure; forming a first **insulating** layer over said gate **dielectric** layer; said first **insulating** layer composed of TEOS oxide, and has a thickness in a range of between about 1000 and 20,000 .ANG.; planarizing said first **dielectric** layer;

b) forming a **second insulating** layer on said first **insulating** layer; said

second insulating layer is composed of PSG; said **second insulating** layer has a thickness less than 0.3 .mu.m; then

c) forming a first photoresist layer on said **second insulating** layer; said first photoresist layer having a first photoresist opening over said contact area; said first photoresist opening has an open dimension in a range of between about 0.15 and 0.5 .mu.m; then

d) etching said **second insulating** layer to form a disk shaped opening; said disk shaped opening having flat bottom comprised of said first **insulating** layer; said disk shaped opening having sidewalls; the etch is an isotropic etch having an etch selectivity between said **second insulating** layer and said first **insulating** layer in a range of between about 2:1 and 20:1; the isotropic etch of said **second insulating** layer comprising buffered oxide etch and the isotropic etch removing a horizontal width of said **second insulating** layer in a range of between about 0.05 and 0.3 .mu.m; then

e) **etching** said gate **dielectric** layer and said **first insulating** layer to form a lower opening; the etch using a dry etch to expose the top surface of said semiconductor structure; a nail shaped contact hole comprised of (a) said disk shaped opening and (b) said lower opening; said lower opening having straight sidewalls;

g) depositing a conductive layer filling said nail shaped contact hole and overlying said **second insulating** layer; said conductive layer is composed of a material selected from the group consisting of polysilicon, W, Al and Ti/TiN, and said conductive layer has a thickness in a range of between about 1000 and 10,000 .ANG.; and

a) providing a metal layer over a semiconductor structure; forming a first **insulating** layer over said metal layer and said semiconductor structure;

b) forming a **second insulating** layer on said first **insulating** layer; said

second insulating layer is composed of PSG; then

c) forming a first photoresist layer on said **second insulating** layer; said first photoresist layer having a first photorestist opening over a contact area; then

d) **etching said second insulating** layer using an isotropic etch forming a disk shaped opening, said disk shaped opening having flat bottom comprised of said **first insulating** layer; said disk shaped opening having sidewalls; the isotropic etch having an etch selectivity between said about 2:1 and 20:1; then

e) **etching said first insulation** layer to form a lower opening; the etch using a anisotropic etch to expose the surface of said metal layer forming a nail shaped contact hole is comprised of (a) said disk shaped opening and (b) said lower opening; said lower opening having straight sidewalls; then

g) depositing a conductive layer filling said nail shaped contact hole and overlying said **second insulating** layer; and

a) forming a first **insulating** layer over a semiconductor structure;

b) planarizing said first **insulating** layer;

c) forming a **second insulating** layer on said first **insulating** layer; said **second insulating** layer is composed of PSG;

d) forming a first photoresist layer on said **second insulating** layer; said first photoresist layer having a first photoresist opening over said contact area; then

e) **etching said second insulating** layer using an isotropic etch forming a disk shaped opening, said disk shaped opening having flat bottom comprised of said

first insulating layer; said disk shaped opening having vertical sidewalls; then

f) **etching said first insulating** layer using a anisotropic etch to expose the surface of said semiconductor structure to form a lower opening; said lower opening and said disk shape opening comprise a nail shaped contact hole; then

h) depositing a conductive layer filling said nail shaped contact hole and overlying said **second insulating** layer; and

j) forming a third **insulating** layer on said first nail shaped conductive plug and said **second insulating** layer;

k) forming a fourth **insulating** layer on said third **insulating** layer; said fourth **insulating** layer composed of PSG;

l) forming a **second** photoresist layer on said fourth **insulating** layer; said **second** photoresist layer having a **second** photoresist opening over said first nail shaped conductive plug; then

m) **etching** said fourth **insulating** layer using an isotropic etch forming a **second** disk shaped opening, said **second** disk shaped opening having flat bottom comprised of the planarized said **first insulating** layer; said **second** disk shaped opening has sidewalls; then

n) etching said third **insulating** layer using an anisotropic etch to expose the surface of said first nail shaped conductive plug forming a **second** lower opening; a **second** nail shaped contact hole is comprised of said **second** lower opening and said **second** disk shaped opening; said **second** lower opening have flat sidewalls; then

o) removing said **second** photoresist layer; then

p) depositing a **second** conductive layer filling said **second** nail shaped contact hole and overlying said fourth **insulating** layer; and

q) planarizing said **second** conductive layer thereby forming a **second** nail shaped conductive plug.

11. The method of claim 1 wherein said **second insulating** layer has a thickness less than 0.3 .mu.m.

12. The method of claim 9 wherein said **second insulating** layer has a thickness less than 0.3 .mu.m.

13. The method of claim 10 wherein said **second insulating** layer has a thickness less than 0.3 .mu.m.